ABSTRACT OF THE DISCLOSURE

An integrated circuit is described which include a stored program processor for test and debug of user-definable logic plus external interface between the test/debug circuits and the component pins. The external interface may be via an existing test interface, or a separate serial or parallel port. Test and debug circuits may contain scan strings that may be used to observe states in user-definable logic or be used to provide pseudo-random bit sequences to user-definable logic. Test and debug circuits may also contain on-chip logic analyzer for capturing sequences of logic states in user-definable circuits. Test and debug circuits may be designed to observe states in user-definable circuits during the normal system operation of said user-definable circuits.